The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC600

32/16 Digital Inputs (24V)

Version 1.0

User Manual

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TPMC600-10

32 digital inputs front panel I/O

TPMC600-11

16 digital inputs front panel I/O

TPMC600-20

32 digital inputs P14 I/O

TPMC600-21

16 digital inputs P14 I/O

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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1 Product Description

The TPMC600 is a PMC compatible module and has 32 digital inputs galvanically isolated by optocoupler. The individual inputs are potential free in relation to each other. A high performance input circuit ensures a defined switching point and polarization protection against confusing the pole. All inputs have an electronic debounce circuit with a freely programmable debounce time.

A version with 16 inputs is available as TPMC600-11. All inputs can generate an interrupt. The signal edge handling is programmable.

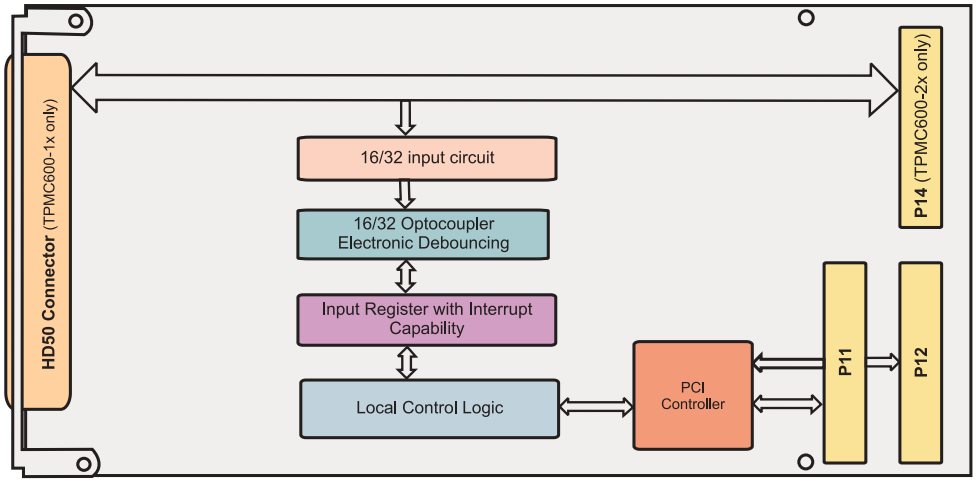

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size	
Electrical Interface	PCI Rev. 2.1 compliant 33MHz / 32 bit PCI 5V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip	PCI9050 (PLX Technology)	
Number of Channels	TPMC600-10/-20: 32 digital inputs TPMC600-11/21: 16 digital inputs	
Input Isolation	Optocoupler for galvanic isolation; also isolated to each other in groups of four inputs	
Input Voltage	24V DC typical	
Input Current	4.2mA typical @ 24V input voltage	
Input Switching Level	2V typical, 7.5V minimum, 14V maximum	
Input Signal Debouncing	Electronic debouncing (7µs to 440ms in steps of 7µs), common for all input channels, can be disabled	
Input Interrupts	32/16 input interrupts (trigger on rising, falling or both edges)	
I/O Interface		
I/O Connector	TPMC600-10/-11: HD50 connector TPMC600-20/-21: PMC P14 I/O (64 pin Mezzanine Connector)	
Physical Data		
Power Requirements	250mA typical @+5V DC	
Temperature Range	Operating Storage	-40 °C to +85 °C -55°C to +125°C
MTBF	TPMC600-10/-20: 208020 h TPMC600-11/-21: 313610 h	
Humidity	5 – 95 % non-condensing	
Weight	74 g	

Figure 2-1 : Technical Specification

3 Local Space Addressing

3.1 PCI9050 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9050 local spaces.

PCI9050 Local Space	PCI9050 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	0 (0x10)	MEM	128	32	LITTLE	Local Configuration Registers
1	1(0x14)	I/O	128	32	LITTLE	Local Configuration Registers
2	2 (0x18)	MEM	32	32	BIG	Local Address Space 0
3	3 (0x1C)	-	-	-	-	Local Address Space 1
4	4 (0x20)	-	-	-	-	Local Address Space 2
5	5 (0x24)	-	-	-	-	Local Address Space 3
6	6 (0x30)	-	-	-	-	Local Expansion ROM Space

Figure 3-1 : PCI9050 Local Space Configuration

3.2 Local Register Space 1

PCI Base Address: PCI9050 PCI Base Address 2 (Offset 0x18 in PCI Configuration Space).

Offset to PCI Base Address 2	Register Name	Access	Size (Bit)
0x0000	Data Input	R	32
0x0004	Control	R/W	32
0x0008	Rising Edge Interrupt Enable	R/W	32
0x000C	Falling Edge Interrupt Enable	R/W	32
0x0010	Rising Edge Interrupt Status	R/W	32
0x0014	Falling Edge Interrupt Status	R/W	32
0x0018	Debounce Time	R/W	32

Figure 3-2 : Local Register Space 1

After power-on or reset all read/write registers are cleared to ‘0’.

3.2.1 Data Input Register

The Data Input Register is a 32 bit wide read only register that reflects the actual status of the inputs.

Bit	Symbol	Description	Access	Reset Value
31:0		32 bit Input Data Bit 0 represents INPUT 1 and bit 31 represents INPUT32.	R	

Figure 3-3 : Data Input Register

3.2.2 Control Register

The Control Register is a read/write register.

Bit	Symbol	Description	Access	Reset Value
31:3		Not used and undefined during reads		
2		Debounce Enable bit 1 = enables the debounce function for all 32 inputs 0 = disable	R/W	
1		Not used		
0		Global Interrupt Enable bit 1 = enables interrupt for all 32 inputs 0 = disable The input channels generate interrupts at pin INTA# of the PCI bus	R/W	

Figure 3-4 : Control Register

Additional to this Global Interrupt Enable the Interrupt INTA# must be enabled in the Interrupt Control/Status Register (INTCSR; 0x4C) of the PCI Controller PCI9050-1. Default after power-on or reset: INTA# is enabled.

3.2.3 Rising Edge Interrupt Enable Register

The Rising Edge Interrupt Enable Register is a 32 bit wide read/write register.

Bit	Symbol	Description	Access	Reset Value
31:0		Bit 0 enables the interrupt of input channel 1 for the rising edge, bit 31 enables interrupt of input channel 32. All other bits are equivalent. 1 = Interrupt Rising Edge enabled 0 = Interrupt Rising Edge disabled	R/W	

Figure 3-5 : Rising Edge Interrupt Enable Register

3.2.4 Falling Edge Interrupt Enable Register

The Falling Edge Interrupt Enable Register is a 32 bit wide read/write register.

Bit	Symbol	Description	Access	Reset Value
31:0		Bit 0 enables the interrupt of input channel 1 for the falling edge, bit 31 enables interrupt of input channel 32. All other bits are equivalent. 1 = Interrupt Falling Edge enabled 0 = Interrupt Falling Edge disabled	R/W	

Figure 3-6 : Falling Edge Interrupt Enable Register

3.2.5 Rising Edge Interrupt Status Register

The Rising Edge Status Enable Register is a 32 bit wide read/write register.

Bit	Symbol	Description	Access	Reset Value
31:0		Bit 0 reflects the interrupt request status of input 1 for the rising edge, bit 31 reflects the interrupt request status of input 31. All other bits are equivalent. 1 = Interrupt request pending 0 = No interrupt request pending Writing '1' to clear an interrupt request of a specific input.	R/W	

Figure 3-7 : Rising Edge Interrupt Status Register

3.2.6 Falling Edge Interrupt Status Register

The Falling Edge Status Enable Register is a 32 bit wide read/write register.

Bit	Symbol	Description	Access	Reset Value
31:0		Bit 0 reflects the interrupt request status of input 1 for the falling edge, bit 31 reflects the interrupt request status of input 31. All other bits are equivalent. 1 = Interrupt request pending 0 = No interrupt request pending Writing '1' to clear an interrupt request of a specific input.	R/W	

Figure 3-8 : Falling Edge Interrupt Status Register

3.2.7 Debounce Time Register

Typ. Debounce Time [ms]	Inaccuracy [ms]	Counter dez.	Counter hex.
0.007	± 0.001	0	0000
0.014	± 0.002	1	0001
0.021	± 0.003	2	0002
0.027	± 0.004	3	0003
0.034	± 0.005	4	0004
0.041	± 0.006	5	0005
0.050	± 0.007	6	0006
0.060	± 0.008	7	0007
0.070	± 0.010	9	0009
0.080	± 0.011	10	000A
0.090	± 0.012	12	000C
0.100	± 0.013	13	000D
0.200	± 0.028	28	001C
0.300	± 0042	43	002B
0.400	± 0.057	58	003A
0.500	± 0.071	73	0049
0.600	± 0.085	88	0058
0.700	± 0.100	103	0067
0.800	± 0.114	118	0076
0.900	± 0.128	132	0084
1.000	± 0.142	147	0093
2.000	± 0.285	296	0128
3.000	± 0.428	445	01BD
4.000	± 0.571	594	0252
5.000	± 0.714	743	02E7
6.000	± 0.856	891	037B
7.000	± 0.999	1040	0410
8.000	± 1.142	1189	04A5
9.000	± 1.285	1338	053A
10.000	± 1.428	1487	05CF
20.000	± 2.857	2975	0B9F
50.000	± 7.142	7439	1D0F
100.000	± 14.285	14879	3A1F
200.000	± 28.571	29760	7440
250.000	± 35.714	37201	9151
300.000	± 42.856	44641	AE61

Typ. Debounce Time [ms]	Inaccuracy [ms]	Counter dez.	Counter hex.
350.000	± 50.000	52082	CB72
400.000	± 57.142	59522	E882
440.402	± 62.915	65535	FFFF

Figure 3-11: Debounce Time / Examples

4 PCI9050 Target Chip

4.1 PCI Configuration Registers (PCR)

4.1.1 PCI9050 Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	0258 1498
0x04	Status		Command		Y	0280 0000
0x08	Class Code			Revision ID	N	11800000
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers				Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers				Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0				Y	FFFFFFE0
0x1C	PCI Base Address 3 for Local Address Space 1				Y	00000000
0x20	PCI Base Address 4 for Local Address Space 2				Y	00000000
0x24	PCI Base Address 5 for Local Address Space 3				Y	00000000
0x28	PCI Cardbus Information Structure Pointer				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	000A 1498
0x30	PCI Base Address for Local Expansion ROM				Y	00000000
0x34	Reserved				N	00000000
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00

Figure 4-1 : PCI9050 Header TPMC600-10

4.1.2 PCI Base Address Initialization

PCI Base Address Initialization is scope of the PCI host software.

PCI9050 PCI Base Address Initialization:

- Write 0xFFFF_FFFF to the PCI9050 PCI Base Address Register.
- Read back the PCI9050 PCI Base Address Register.
- For PCI Base Address Registers 0:5, check bit 0 for PCI Address Space:

  Bit 0 = '0' requires PCI Memory Space mapping

  Bit 0 = '1' requires PCI I/O Space mapping

  For the PCI Expansion ROM Base Address Register, check bit 0 for usage:

  Bit 0 = ‘0’: Expansion ROM not used

  Bit 0 = ‘1’: Expansion ROM used

- Or PCI I/O Space mapping, starting at bit location 2, the first bit set determines the size of the required PCI I/O Space size.

  For PCI Memory Space mapping, starting at bit location 4, the first bit set to '1' determines the size of the required PCI Memory Space size.

  For PCI Expansion ROM mapping, starting at bit location 11, the first bit set to '1' determines the required PCI Expansion ROM size.

  For example, if bit 5 of a PCI Base Address Register is detected as the first bit set to ‘1’, the PCI 9050 is requesting a 32 byte space (address bits 4:0 are not part of base address decoding).

- Determine the base address and write the base address to the PCI9050 PCI Base Address Register. For PCI Memory Space mapping the mapped address region must comply with the definition of bits 3:1 of the PCI9050 PCI Base Address Register.

  After programming the PCI9050 PCI Base Address Registers, the software must enable the PCI9050 for PCI I/O and/or PCI Memory Space access in the PCI9050 PCI Command Register (Offset 0x04). To enable PCI I/O Space access to the PCI9050, set bit 0 to '1'. To enable PCI Memory Space access to the PCI9050, set bit 1 to '1'.

For further information please refer to the PCI9050 manual which is part of the TPMC600-ED Engineering Documentation.

4.2 Local Configuration Register (LCR)

After reset, the PCI9050 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

The PCI base address for the PCI9050 Local Configuration Registers is PCI9050 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9050 PCI Configuration Register Space) or PCI9050 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9050 PCI Configuration Register Space).

Do not change hardware dependent bit settings in the PCI9050 Local Configuration Registers.

PCI (Offset from Local Base Address)	Register	Value
0x00	Local Address Space 0 Range	0x0FFFFFE0
0x04	Local Address Space 1 Range	0x00000000
0x08	Local Address Space 2 Range	0x00000000
0x0C	Local Address Space 3 Range	0x00000000
0x10	Local Exp. ROM Range	0x00000000
0x14	Local Re-map Register Space 0	0x00000001
0x18	Local Re-map Register Space 1	0x00000000
0x1C	Local Re-map Register Space 2	0x00000000
0x20	Local Re-map Register Space 3	0x00000000
0x24	Local Re-map Register ROM	0x00000000
0x28	Local Address Space 0 Descriptor	0x01B17880
0x2C	Local Address Space 1 Descriptor	0x00000000
0x30	Local Address Space 2 Descriptor	0x00000000
0x34	Local Address Space 3 Descriptor	0x00000000
0x38	Local Exp. ROM Descriptor	0x00000000
0x3C	Chip Select 0 Base Address	0x00000011
0x40	Chip Select 1 Base Address	0x00000000
0x44	Chip Select 2 Base Address	0x00000000
0x48	Chip Select 3 Base Address	0x00000000
0x4C	Interrupt Control/Status	0x00000041
0x50	Miscellaneous Control Register	0x00780000

Figure 4-2 : Local Configuration Register

4.3 Configuration EEPROM

After power-on or PCI reset, the PCI9050 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x0F : PCI9050 PCI Configuration Register Values
- Address 0x10 to 0x64 : PCI9050 Local Configuration Register Values
- Address 0x65 to 0x7C : Not used
- Address 0x7E to 0x7F : TPMC variant

See the PCI9050 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x0258	0x1498	0x1180	0x0000	s.b.	0x1498	0x0000	0x0100
0x10	0x0FFF	0xFFE0	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x20	0x0000	0x0000	0x0000	0x0001	0x0000	0x0000	0x0000	0x0000
0x30	0x0000	0x0000	0x0000	0x0000	0x01B1	0x7880	0x0000	0x0000
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0011
0x50	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0041
0x60	0x0078	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x70	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Figure 4-3 : Configuration EEPROM TPMC600-xx

Subsystem-ID Value (Offset 0x08):

TPMC600-10	0x000A
TPMC600-11	0x000B
TPMC600-20	0x0014
TPMC600-21	0x0015

5 Configuration Hints

5.1 Big / Little Endian

- PCI – Bus (Little Endian)

Byte 0	AD[7..0]
Byte 1	AD[15..8]
Byte 2	AD[23..16]
Byte 3	AD[31..24]

- Every Local Address Space (0...3) and the Expansion ROM Space can be programmed to operate in Big or Little Endian Mode.

Big Endian		**Little Endian**	
32 Bit		**32 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
Byte 2	D[15..8]	Byte 2	D[23..16]
Byte 3	D[7..0]	Byte 3	D[31..24]
16 Bit upper lane		**16 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
16 Bit lower lane			
Byte 0	D[15..8]		
Byte 1	D[7..0]		
8 Bit upper lane		**8 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
8 Bit lower lane			
Byte 0	D[7..0]		

Figure 5-1 : Local Bus Little/Big Endian

Standard use of the TPMC600:

Local Address Space 0	32 bit bus in Big Endian Mode
Local Address Space 1	not used
Local Address Space 2	not used
Local Address Space 3	not used
Expansion ROM Space	not used

To change the Endian Mode use the Local Configuration Registers for the corresponding Space. Bit 24 of the according register sets the mode. A value of 1 indicates Big Endian and a value of 0 indicates Little Endian.

For further information please refer to the PCI9050 manual which is also part of the TPMC600-ED Engineering Documentation.

Use the PCI Base Address 0 + Offset or PCI Base Address 1 + Offset:

Short cut Offset	Name	
LAS0BRD	0x28	Local Address Space 0 Bus Region Description Register
LAS1BRD	0x2C	Local Address Space 0 Bus Region Description Register
LAS2BRD	0x30	Local Address Space 0 Bus Region Description Register
LAS3BRD	0x34	Local Address Space 0 Bus Region Description Register
EROMBRD	0x38	Expansion ROM Bus Region Description Register

You could also use the PCI - Base Address 1 I/O Mapped Configuration Registers.

5.1.1 PCI Interrupt Control/Status Register

All 32 input channels generate interrupts at pin INTA# of the PCI bus. The interrupt status can be read at the Interrupt Status Register INTCSR of the PCI Controller PCI9050-1.

Bit	Description	Access	Reset Value
31:8	unused	R	0
7	Software Interrupt	R/W	0
6	PCI Interrupt Enable	R/W	1
5	Local Interrupt 2 Status	R	0
4	Local Interrupt 2 Polarity	R/W	0
3	Local Interrupt 2 Enable	R/W	0
2	Local Interrupt 1Status	R	0
1	Local Interrupt 1 Polarity	R/W	0
0	Local Interrupt 1 Enable	R/W	1

Figure 5-2 : Interrupt Control/Status Register (INTCSR; 0x4C)

5.2 Software Reset (Controller and LRESET#)

A host on the PCI bus can set the software reset bit in the Miscellaneous Control Register (CNTRL; 0x50) of the PCI Controller PCI9050 to reset the Controller and assert LRESET# output. The PCI9050 remains in this reset condition until the PCI host clears the software reset bit.

6 Functional Description

6.1 Digital Inputs

6.1.1 Optical Isolation

The TPMC600 has 32 (TPMC600-10/-20) or 16 (TPMC600-11/-21) digital inputs. The standard signal level for these inputs is 24V DC. The switching level of the inputs is between 7.5V and 14V. All inputs are isolated by optocoupler from the computer system and are also isolated against each other in groups of four inputs.

Group	Ground	Input
I1	GND_I1	IN 1 IN 2 IN 3 IN 4
I2	GND_I2	IN 5 IN 6 IN 7 IN 8
I3	GND_I3	IN 9 IN 10 IN 11 IN 12
I4	GND_I4	IN 13 IN 14 IN 15 IN 16
I5	GND_I5	IN 17 IN 18 IN 19 IN 20
I6	GND_I6	IN 21 IN 22 IN 23 IN 24
I7	GND_I7	IN 25 IN 26 IN 27 IN 28
I8	GND_I8	IN 29 IN 30 IN 31 IN 32

Figure 6-1 : Isolated Digital Inputs

6.1.2 Debounce Function

A programmable debounce function common for all inputs is implemented on the TPMC600. There is only one debounce time adjustable for all 32 (TPMC600-10/-20) or 16 (TPMC600-11/-21) digital inputs.

If the debounce function is enabled, the input pin must be static for the programmed debounce time before the rising or falling edge is recognized as valid. So only after a correct identification the Data Input Register is updated and an interrupt is generated.

The debounce function is disabled after power-on and reset. The debounce time is set to value '0'.

6.1.3 Interrupt Logic

Interrupt generation can be individually programmed for each channel and input transition. To enable the interrupt after a reset, the Global Interrupt Enable bit in the Control Register must be set to the value '1'. Also the respective bit for rising or falling edge in the Rising Edge / Falling Edge Interrupt Enable Register must be set.

The Global Interrupt Enable bit and also all individually interrupt enable bits are disabled after power-on and reset.

7 Programming Hints

7.1 Local Read/Write

The local register design is developed for a long word (32 bit) read/write access. A byte or word access could be fail.

Use also long word read/write accesses at TPMC600-11/-21.

8 Installation

8.1 Input Wiring

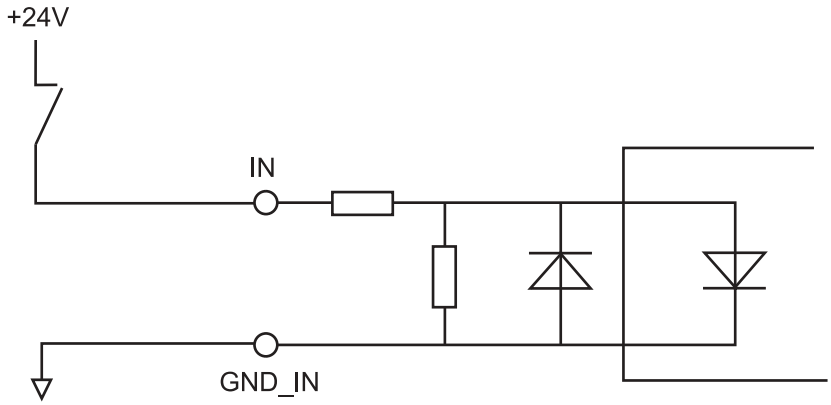

Figure 8-1 : Input Wiring

9 Pin Assignment – I/O Connector

9.1 Front panel I/O

Pin	Signal
1	IN 1
2	IN 2
3	IN 3
4	IN 4
5	IN 5
6	IN 6
7	IN 7
8	IN 8
9	IN 9
10	IN 10
11	IN 11
12	IN 12
13	IN 13
14	IN 14
15	IN 15
16	IN 16
17	IN 17
18	IN 18
19	IN 19
20	IN 10
21	IN 21
22	IN 22
23	IN 23
24	IN 24
25	IN 25

Pin	Signal
26	IN 26
27	IN 27
28	IN 28
29	IN 29
30	IN 30
31	IN 31
32	IN 32
33	GND_I1
34	GND_I2
35	GND_I3
36	GND_I4
37	GND_I5
38	GND_I6
39	GND_I7
40	GND_I8
41	NC
42	NC
43	NC
44	NC
45	NC
46	NC
47	NC
48	NC
49	NC
50	NC

Figure 9-1 : HD50 SCSI-2 type Connector

9.2 Mezzanine Card Connector P14

Pin	Signal
1	IN 1
2	IN 2
3	IN 3
4	IN 4
5	IN 5
6	IN 6
7	IN 7
8	IN 8
9	IN 9
10	IN 10
11	IN 11
12	IN 12
13	IN 13
14	IN 14
15	IN 15
16	IN 16
17	IN 17
18	IN 18
19	IN 19
20	IN 10
21	IN 21

Pin	Signal
22	IN 22
23	IN 23
24	IN 24
25	IN 25
26	IN 26
27	IN 27
28	IN 28
29	IN 29
30	IN 30
31	IN 31
32	IN 32
33	GND_I1
34	GND_I2
35	GND_I3
36	GND_I4
37	GND_I5
38	GND_I6
39	GND_I7
40	GND_I8
41	NC
42…64	NC

Figure 9-2 : Mezzanine Card Connector P14